

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS

The HEF40373B is an 8-bit transparent latch with 3-state buffered outputs. The output stages have high current output capability suitable for driving highly capacitive loads. The latch outputs follow the data inputs when the latch enable (E) is HIGH. When E is LOW, the data that meets the set-up times is latched. The 3-state outputs are controlled by the output enable input \overline{EO} . A HIGH on \overline{EO} causes the outputs to assume a high impedance OFF-state. The device features hysteresis on the E input to improve noise rejection.

Schmitt-trigger action in the E input makes the circuit highly tolerant to slower input rise and fall times.

The HEF40373B is pin and functionally compatible with the TTL '373' device.

Supply voltage range: 3 to 15 V.

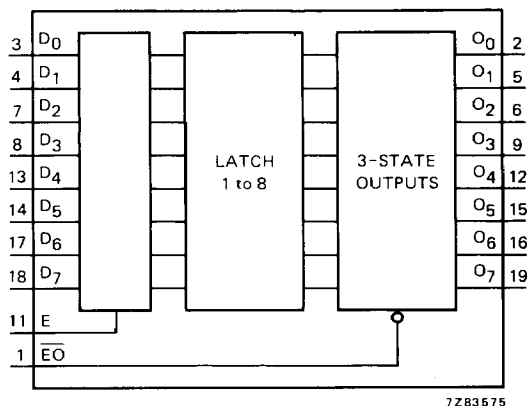


Fig. 1 Functional diagram.

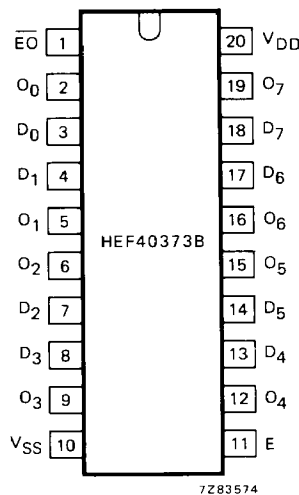


Fig. 2 Pinning diagram.

HEF40373BP : 20-lead DIL; plastic (SOT146).

HEF40373BD: 20-lead DIL; ceramic (cerdip) (SOT152C).

HEF40373BT : 20-lead mini-pack; plastic (SO-20; SOT163A).

PINNING

D_0 to D_7 data inputs
E latch enable input
 \overline{EO} output enable input (active LOW)
 O_0 to O_7 3-state buffered outputs

FAMILY DATA

I_{DD} LIMITS category MSI

see Family Specifications

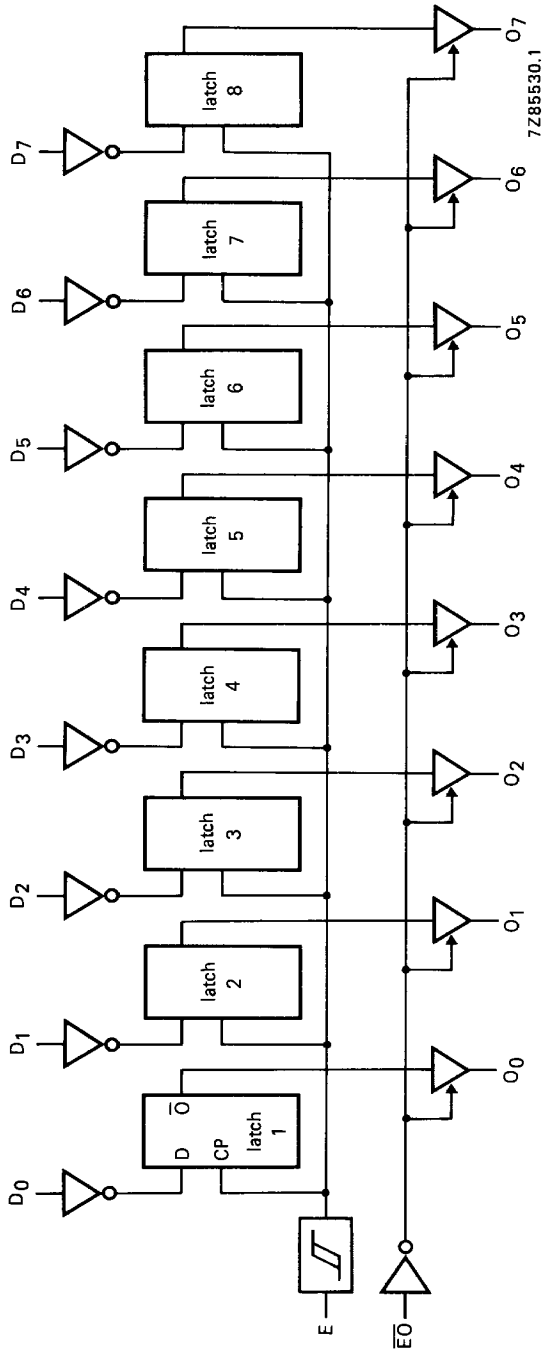


Fig. 3 Logic diagram.

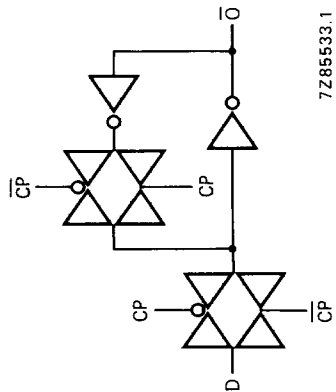


Fig. 4 Logic diagram (one latch).

FUNCTION TABLE

operating modes	inputs			internal register	outputs O ₀ to O ₇
	\overline{EO}	E	D _n		
enable & read register	L	H	L	L	L
	L	H	H	H	H
latch & read register	L	L	l	L	L
	L	L	h	H	H
latch register & disable outputs	H	L	l	L	Z
	H	L	h	H	Z

H = HIGH state (the more positive voltage)

h = HIGH state (one set-up time prior to the HIGH-to-LOW enable transition)

L = LOW state (the less positive voltage)

l = LOW state (one set-up time prior to the HIGH-to-LOW enable transition)

Z = high impedance OFF-state

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

See Family Specifications, except for:

D.C. current into any input	$\pm I_I$	max.	10 mA
D.C. source or sink current into any output	$\pm I_O$	max.	25 mA
D.C. current into the supply terminals	$\pm I$	max.	100 mA

D.C. CHARACTERISTICS

$V_{SS} = 0$ V

	V_{DD} V	V_{OH} V	V_{OL} V	symbol	T_{amb} (°C)					
					-40		+25		+85	
					min.	typ.	min.	typ.	min.	typ.
Output current HIGH	5	4,6		$-I_{OH}$	0,75	0,6	1,2	0,45	mA	
	10	9,5			1,85	1,5	3,0	1,1	mA	
	15	13,5			14,5	15	50	15,5	mA	
Output current HIGH	5	3,6		$-I_{OH}$	9,3	10	24	10,7	mA	
	10	8,4			14,4	15	46	15,0	mA	
	15	13,2			19,5	20	62	19,8	mA	
Output current LOW	5		0,4	I_{OL}	2,9	2,3	5,4	1,75	mA	
	10		0,5		9,5	7,6	17	5,50	mA	
	15		1,5		30,0	25	45	19,0	mA	
Hysteresis voltage at enable input (E)	5			V_H			220		mV	
	10						250		mV	
	15						320		mV	

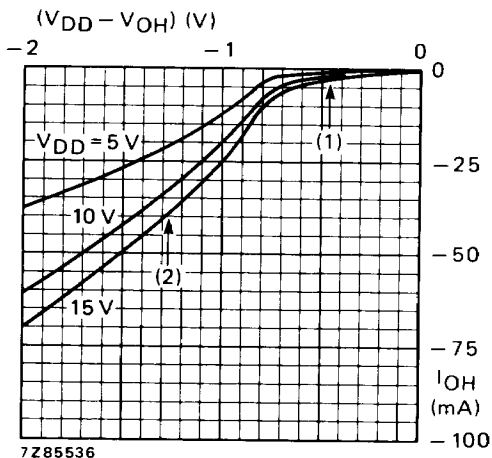


Fig. 5 Typical output source current characteristic.

- (1) P-channel MOS transistor conducting.
- (2) P-channel MOS transistor and bipolar n-p-n transistor conducting.

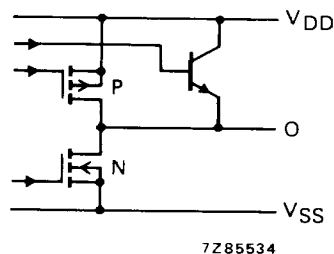


Fig. 6 Schematic diagram of output stage.

A.C. CHARACTERISTICS

 $V_{SS} = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $C_L = 50 \text{ pF}$; input transition times $\leq 20 \text{ ns}$

	V_{DD} V	symbol	min.	typ.	max.	typical extrapolation formula	
Propagation delays							
$E \rightarrow O_n$	5			150	300	ns	$138 \text{ ns} + (0,24 \text{ ns/pF}) C_L$
HIGH to LOW	10	t_{PHL}		60	120	ns	$59 \text{ ns} + (0,01 \text{ ns/pF}) C_L$
	15			40	80	ns	$36 \text{ ns} + (0,07 \text{ ns/pF}) C_L$
$E \rightarrow O_n$	5			125	250	ns	$122 \text{ ns} + (0,06 \text{ ns/pF}) C_L$
LOW to HIGH	10	t_{PLH}		50	100	ns	$48 \text{ ns} + (0,03 \text{ ns/pF}) C_L$
	15			40	80	ns	$39 \text{ ns} + (0,02 \text{ ns/pF}) C_L$
Output transition times	5			40	80	ns	see Fig. 7.
HIGH to LOW	10	t_{THL}		20	40	ns	
	15			15	30	ns	
LOW to HIGH	5			30	60	ns	
	10	t_{TLH}		20	40	ns	
	15			15	30	ns	
3-state propagation delays							
Output disable times							
$\overline{E}O \rightarrow O_n$	5			65	130	ns	t_{PHZ}
HIGH	10			30	60	ns	
	15			25	50	ns	
LOW	5			75	150	ns	t_{PLZ}
	10			40	80	ns	
	15			30	60	ns	
Output enable times							
$\overline{E}O \rightarrow O_n$	5			65	130	ns	t_{PZH}
HIGH	10			30	60	ns	
	15			25	50	ns	
LOW	5			85	170	ns	t_{PZL}
	10			35	70	ns	
	15			25	50	ns	
Set-up time	5		15	7		ns	t_{su}
$D_n \rightarrow E$	10		10	5		ns	
	15		10	5		ns	
Hold time	5		25	15		ns	t_{hold}
$D_n \rightarrow E$	10		15	4		ns	
	15		10	3		ns	
Minimum latch enable pulse width LOW	5		60	30		ns	t_{WEL}
	10		30	15		ns	
	15		20	10		ns	

A.C. CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V _{DD} V	typical formula for P (μW)	where f _i = input freq. (MHz) f _o = output freq. (MHz) C _L = load capacitance (pF) Σ(f _o C _L) = sum of outputs V _{DD} = supply voltage (V)
Dynamic power dissipation per package (P)	5	$3\,325 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	10	$14\,200 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	
	15	$37\,425 f_i + \Sigma(f_o C_L) \times V_{DD}^2$	

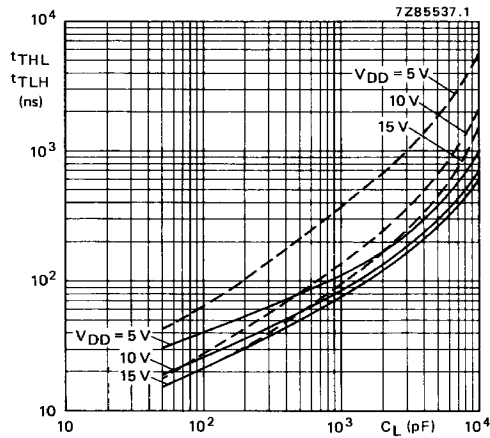


Fig. 7 Output transition times as a function of the load capacitance.

— t_{TLH}; - - - t_{THL}.